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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

MCLEAN MAYO, KIMBERLY N

ART UNIT	PAPER NUMBER
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2187

DATE MAILED: 12/04/2003

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/965,387

Applicant(s)

COSKY ET AL.

Examiner

Kimberly N. McLean-Mayo

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 September 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-43 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-43 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on September 8, 2003 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-2 and 20-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Tung (USPN: 5,854,638).

Regarding claims 1 and 20, Tung discloses initializing a circuit, (Figure 1, Reference 126; inherently the circuit is initialized as all circuits are initialized during power-up [reset] to a particular state), the circuit having at least one memory element coupled to a memory bus on a host system (Figure 1, Reference 150); monitoring signals on the memory bus and detecting a first sequence of signals, the first sequence of signals including a reserved memory address

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(reserved memory address is an address within the address range of the memory bank reserved for shared access by the video controller and the host; C 2, L 49-65; Figure 1, Reference 150; C 3, L 50-53)(the host controller monitors the memory bus and detects when the request is for the shared bank or the exclusive bank and thus the host controller detects a first sequence of signals including a reserved memory address; C 5, L 29-67; C 6, L 1-53; the video arbitration circuit monitors and detects signals on the memory bus by monitoring request signals vlpr, vhpr and thus when a request signal is asserted within the video controller a first sequence of signals including a reserved memory address is detected; C 13, L 36-60;); switching control of the at least one memory element to the circuit in response to detection of the reserved memory address (C 12, L 45-67). Additionally with respect to claim 20, hardware system elements are intrinsically controlled by software such as device drivers, microcode, etc. and thus it is evident that the system above comprises a machine-accessible medium including instructions, that when executed by the machine, causes the machine to perform the operations above.

Regarding claims 2 and 21, detecting a second sequence of signals, the second sequence of signals including another reserved memory address (a memory request from the host to an address within the reserved address range of the shared bank memory) and switching control of the at least one memory element to the host system in response to detection of the another reserved memory address (C 12, L 45-67).

4. Claim 1-41 are rejected under 35 U.S.C. 102(e) as being anticipated by Moyer (PGPUB: 2002/0199052 A1)

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Regarding claims 1, 9-10, 20, 28-31 and 34-35, Moyer discloses initializing a circuit (Page 3, Section [0022], lines 22-32, lines 53-61 - the circuit is initialized by storing arbitration policies in control registers, References 56, 62, 63, 64 and 65 in Figure 4; Page 2, Section [0021], lines 30 +), wherein the circuit has at least one memory element coupled to a memory bus (Figure 1, Reference 12) on a host system (Figure 1, Reference 14 – host system)(the circuit is comprised of References 34, 36, 38, 40, 20, 22 and 24); monitoring signals on the memory bus (Page 2, Section [0021], lines 1-20 – the signals are monitored on the bus via input 12 in Figure 4); detecting [identifying] a first sequence of signals including a reserved memory address (the first sequence of signals comprises the address signals corresponding the memory request [section 0022, lines 8-15], the signals corresponding to Reference 53 in Figure 4 [section 0022, lines 41-42], the signals corresponding to Reference 56 in Figure 4 [section 0022, lines 41-42]) [the reserved memory address is any address corresponding to memory elements 20, 22 and 24 in Figure 1; the circuit monitors by receiving memory request to access the memory element and thus the circuit effectively monitors the memory addresses corresponding to the memory element] and switching control of the at least one memory element to the circuit in response to detection of the reserved memory address (Page 3, Section [0022], lines 11-15, lines 38-49 – the logic circuit receives one or more bus requests [memory address] and in response to receiving such request switches control of the memory element based on some predetermined criteria such as the current transfer type signal). Additionally with respect to claim 20, hardware system elements are intrinsically controlled by software such as device drivers, microcode, etc. and thus it is evident that the system above comprises a machine-accessible medium including

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instructions, that when executed by the machine, causes the machine to perform the operations above.

Regarding claims 2-3 and 21-22, Moyer discloses detecting a second sequence of signals including another reserved memory address and switching control of the at least one memory element to the host system in response to detection of another reserved memory address (Page 3, Section [0022], lines 38-49 – when the information monitored and retrieved from the control register(s) indicated that the host system should be granted access to the bus).

Regarding claims 4 and 23, Moyer discloses initializing a circuit having at least one memory element coupled to a memory bus on a host system comprising detecting a sequence of writes to memory locations on the circuit (Page 3, Section [0022], lines 22-32, lines 53-61; Page 2, Section [0021], lines 30 +; logic within Reference 34 for identifying when information is being written to the control registers, References 56, 62, 63, 64 and 65 in Figure 4).

Regarding claims 5 and 24, Moyer discloses the sequence of writes as writes to random memory locations (locations of the configuration registers).

Regarding claims 6-8 and 25-27, Moyer discloses monitoring signals on the memory bus comprising the circuit monitoring control, address and data signals on the host system (Page 2, Section [0021], lines 7-20).

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Regarding claims 11, 18-19 and 32-33, Moyer discloses a memory bus on a host system (Figure 1, Reference 12); a plurality of memory elements on a circuit, (the circuit is comprised References 34, 36, 38, 40, 20, 22 and 24), the plurality of memory elements communicatively coupled with the memory bus (the plurality of memory elements – Figure 1, References 20, 22 and 24); a processing element on the circuit communicatively coupled with the plurality of memory elements and the memory bus, the (Figure 1, Reference 34), the processing element to monitor signals on the memory bus (Page 2, Section [0021], lines 1-20 – the signals are monitored on the bus via input 12 in Figure 4); detecting [identifying] a first sequence of signals including a reserved memory address (the first sequence of signals comprises the address signals corresponding the memory request [section 0022, lines 8-15], the signals corresponding to Reference 53 in Figure 4 [section 0022, lines 41-42], the signals corresponding to Reference 56 in Figure 4 [section 0022, lines 41-42]) [the reserved memory address is any address corresponding to the system memory, the circuit monitors by receiving memory request to access the memory element and thus the circuit effectively monitors the memory addresses corresponding to the memory element] and switching control of the at least one memory element to the circuit in response to detection of the reserved memory address (Page 3, Section [0022], lines 38-49).

Claims 12-13 are rejected for the same rationale applied to claims 2-3 above.

Claim 14 is rejected for the same rationale applied to claim 4 above.

Claim 15 is rejected for the same rationale applied to claim 5 above.

Claims 16-18 are rejected for the same rationale applied to claim 6-8 above.

Regarding claims 36-40, Moyer discloses monitoring signals on a memory bus (Figure 1, Reference 12), the memory bus coupled with a memory (any one of References 20, 22 and 24) and a first processor (Figure 1, Reference 14) (Page 2, Section [0021], lines 1-20 – the signals are monitored on the bus via input 12 in Figure 4); and in response to detecting [identifying] a reserved memory address (address corresponding to the memory request, wherein a memory request is a read or write request, [section 0022, lines 8-15]; the reserved memory address is any address corresponding to memory elements 20, 22 and 24 in Figure 1, the circuit monitors by receiving memory request to access the memory element and thus the circuit effectively monitors the memory addresses corresponding to the memory element), switching control of the memory from the first processor to a second processor coupled with the memory bus (a processor is a bus master; any one of References 36, 38 and 40 in Figure 1)(Page 3, Section [0022], lines 38-49 - when the information monitored and retrieved from the control register(s) indicates that the second processor should be granted access to the bus) and in response to detecting another reserved memory address on the memory bus, switching control of the memory from the second processor to the first processor (Page 3, Section [0022], lines 38-49 - when the information monitored and retrieved from the control register(s) indicates that the first processor should be granted access to the bus).

Regarding claim 41, Moyer discloses the memory and the second processor comprising part of a single component (the single component is Reference 10 in Figure 1, a data processing system).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 42-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moyer (PGPUB: 2002/0199052).

Moyer does not explicitly disclose the memory comprising a SDRAM and does not disclose the single component comprising a DIMM coupled with the memory bus. However, it is well known in the art to use SDRAM memories, which provide fast memory access via burst mode operations and dual bank structure. Additionally, it is well known in the art to use DIMMs in a system to provide increased memory storage capacity. Hence, it would have been obvious to one of ordinary skill in the art to provide these features in the system taught by Moyer for the desirable purpose of increased storage capacity and fast memory access.

Response to Arguments

7. Applicant's arguments filed have been fully considered but they are not persuasive. Regarding Applicant's argument that Moyer does not switching control of the memory element in response to detecting the first reserved memory address, the Examiner disagrees. Moyer teaches the logic circuit receiving one or more bus requests [requests to memory addresses] and in response to receiving such requests, the logic circuit switches control of the memory element based on some predetermined criteria such as the current transfer type signal. However, the

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switching is still upon detection of the reserved memory address [address within the bus request] (Page 3, Section [0022], lines 11-15, lines 38-49).

Regarding Applicant's argument regarding the interpretation of reserved memory address, the Examiner has interpreted a reserved memory address as any address corresponding to memory elements 20, 22 and 24 in Figure 1. Each of the memories is a different type of memory and thus each type of memory is mapped to a certain range of addresses within the address space of the system, wherein the mapped range of addresses for each type of memory is reserved for that specific type of memory. This is a conventional interpretation of reserved addresses. Computing systems include an address space, which is divided between the elements in the system thereby reserving those addresses to its corresponding element.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly N. McLean-Mayo whose telephone number is 703-308-9592. The examiner can normally be reached on M-F (9:00 - 6:30) First Friday Off.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 703-308-1756. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7329 for regular communications and 703-746-7240 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-2100.

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KIMBERLY MCLEAN-MAYO
PRIMARY EXAMINER

Kimberly N. McLean-Mayo
Examiner
Art Unit 2187

KNM

December 1, 2003